REMARKS

Claims 1-2 were pending in the application. Claims 1-2 have been amended. Claims 3-10 are newly submitted. The specification has been amended to correspond with the Figures and the Figures have been amended to correspond with the specification. In addition minor informalities have been corrected in the specification. No new matter has been added. Claims 1-10 are now pending in the application. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. Drawings

The drawings were objected to under 37 CFR 1.83(a) as not showing every claimed feature. Specifically, the Examiner noted that the fractionally spaced transversal filter recited in claim 2 must be shown. Applicant has amended FIG. 2 to include a reference number 18 to designate a fractionally spaced transversal filter as described in the specification. Applicant, therefore, respectfully requests withdrawal of the objections to the drawings.

II. The § 112 Rejections

Claims 1 and 2 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. With regard to the limitation "the recovered clock signal is independent of the equalization" in claim 1, the Examiner asserts that the specification does not describe any specific means of clock recovery or clock recovery independent of equalization. Although claim 1 has been amended to delete this limitation, Applicant respectfully disagrees with the Examiner's assertion.

As described in the background of Applicant's specification, in a conventional DSP equalizer, tap values (or intermediate signal values at the output of a delay stage of the equalizer) must be known. In order to determine tap values, the timing of data must be recovered before, or at the same time as equalization. Specification, page 1, lines 15-20. In contrast, in one implementation of the present invention, tap values do not need to be known for adjustment of the tap values (or coefficients) and, therefore, equalization can be performed independent of any timing recovery.

Claims 1 and 2 have also been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant has amended the claims to provide sufficient antecedent basis for all limitations.

III. The §102 Rejections

Claims 1-2 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication No. 2001/0043650 ("Sommer").

Applicant respectfully traverses the rejection.

Claim 1, as amended, recites an adaptive equalizer for equalizing a signal. The adaptive equalizer includes a convergence algorithm circuit to adjust coefficients associated with a feed-forward equalizer (FFE) based on error measured in a partially equalized signal by a signal quality circuit. Values of the coefficient are not used by the convergence algorithm circuit to adjust of the coefficients associated with the feed-forward equalizer (FFE).

A. Sommer Fails To Disclose a Convergence Algorithm Circuit to Adjust Coefficients Associated With a Feed-Forward Equalizer in Which Values of

the Coefficients Are Not Used by the Convergence Algorithm Circuit to Adjust the Coefficients Associated With the Feed-Forward Equalizer

Sommer discloses an adaptive equalizer capable of tracking rapid channel variations while maintaining high stability and low jitter (see Abstract). To this end, the adaptive equalizer includes an equalizer controller 30 that functions to sense the rate change of coefficients in each of the FFE and DFE sections of the adaptive equalizer, and increase or decrease step size parameters of the section accordingly, and if the controller senses a high gradient magnitudes from one or more FFE or DFE sections, the controller adjusts the step sizes of those sections to allow fast adjustment of those sections. In addition, the controller monitors the tap coefficients of the each FFE and DFE section, detects a time variation of the tap coefficients, and adjusts step sizes of those sections with a large time variation so as to permit fast adjustment of the tap coefficients. See paragraph [0058].

While Sommer discloses an adaptive equalizer that adjusts tap coefficients of one or more FFE sections to track rapid channel variations, Sommer nevertheless fails to disclose a convergence algorithm circuit to adjust coefficients associated with a feed-forward equalizer in which values of the coefficients are not used by the convergence algorithm circuit to adjust the coefficients associated with the feed-forward equalizer, as required in claim 1. Instead (as discussed above), in order to provide a fast adjustment, the controller 30 in Sommer's adapative equalizer monitors the tap coefficients of each FFE and DFE section and adjusts step sizes of those sections that have a large time variation. Consequently, Sommer's technique for adjusting the tap coefficients of each FFE and DFE section requires knowledge of values associated with the tap coefficients.

For at least these reasons, Applicant submits that claim 1 (and the claims that depend therefrom) are allowable over Sommer.

B. Other Independent Claims

Claim 8 incorporates limitations similar to those of claim 1. Claim 8 (and the claims that depend therefrom) are also allowable over Sommer for reasons corresponding to those set forth with respect to claim 1.

Applicant submits that claims 1-10 are allowable over Sommer. Should any unresolved issues remain, Examiner is invited to call the undersigned at the telephone number indicated below.

Respectfully submitted,
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